WT-QSFP28-AOC-XX

QSFP28 100G Active Optical Cable

1. Feature

- RoHS-6 compliant
- Support parallel optics 4x25.78 Gbps operation
- Compliant to MSA standard SFF-8665
- Total power consumption less than 3.5W per end
- Hot-pluggable, light weight cable, small bending radius and reach up to 70m(OM3)/100m(OM4)
- IEEE802.3bm CAUI-4 electrical compatibility
- I2C standard management interface
- 0 to 70 °C case temperature

2. Description

The WT-QSFP28-AOC-XX is a 100Gbps, hot pluggable active optical cable for InfiniBand EDR and Ethernet data transmission. It provides full duplex, parallel interconnects: 4 transmitting and 4 receiving data lanes and supports distance up to 100 meters.

The QAOC-10G4F1Axx is composed of multi-channel optical transceivers in both ends and multimode fiber cable in between. This integrated optical module solution removes the complicated optical fiber interface and brings friendly and intuitive electrical-to-electrical interface to users.

WT-QSFP28-AOC-XX is designed to meet the requirements of high speed, high density and low power consumption for applications in today's data centers.

3. Application

- □ 100G Ethernet (100GBASE-SR4)
- □ InfiniBand EDR (4x25.78bps)
- □ Proprietary high speed, high density data transmission.
- □ Switch and router high speed backplane interconnect
- □ High performance computing, server and data storage

4. Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Units	Notes
Storage Temperature	T_S	-40		70	°C	
Storage Ambient Humidity	H_A	0		85	%	
+3.3V Power Supply	V_{CC33}	0	3.3	3.6	V	

5. General Operating Characteristics

Parameter	Symbol	Min	Typ	Max	Units	Notes
Operating Case Temperature	TC	0		70	°C	
Ambient Humidity	HA	5		85	%	[1]
+3.3V Supply Voltage	V_{CC33}	3.135	3.3	3.465	V	
Total Power Dissipation	PD			3.5	W	Per End
Bit Rate	BR	-100_{ppm}	25.78125	$+100_{ppm}$	Gb/s	[2]
Module Turn-on				2000	ms	[3]

Time						
Input Control Voltage- High	VIH	2.0		V_{CC33}+0.3	V	[4]
Input Control Voltage - Low	VIL	-0.3		0.8	V	[4]
Digital Output Voltage- High	VOH	V_{CC33}-0.5		V_{CC33}+0.3		[5]
Digital Output Voltage- Low	VOL	0		0.4		[5]
Clock Rate-I2C				400	KHz	[6]

Notes:

1. Non-condensing
2. Test with PRBS 2^{31}-1, BER=1x10^{-12}
3. Time from module power-on / insertion/ ResetL deassert to module full functional.
4. For all control input pins: LPMode, Reset and ModSelL
5. For all status output pins: ModPrsL, IntL
6. For management interface

6. Electrical Input Characteristics

(V_{CC33} = 3.135V ~ 3.465V, T_C= 0 º to 70 ºC, per end)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential Input Impedance	Zdiff	90	100	110	Ω	
Differential Input Return Loss	SDD11	[1]			dB	0.01 to 19 GHz
Differential to Common Mode Input Return Loss	SCD11	[2]			dB	0.01 to 19 GHz
Differential Data Input Swing	Vin_pp	900			mV	TP1

Notes:

1. SDD11≥9.5–0.37f.,when 0.01≤f<8 ;SDD11≥ 4.75–.7.4log$_{10}$(.f/14), when 8≤f<19

2. .SCD11≥22–20(f / 25.78),when 0.01≤f<12.89 ; SDC11≥15–6(f / 25.78),when 12.89≤f<19

7. Electrical Output Characteristics

(V_{CC33} = 3.135V ~ 3.465V, T_C= 0 ºC to 70 º, per end)

Parameter	Symbol	Min	Typ	Max	Units	Notes
Differential Output Impedance	Zdiff	90	100	110	Ω	
Output Transition (Rise/Fall) Time (20% to 80%)	tr/tf	12			ps	
AC Common-Mode Output Voltage				17.5	mV	RMS
Differential Output Return Loss	SDD22	[1]			dB	0.01 to 19 GHz
Common to Differential Mode Input Return Loss	SDC22	[2]			dB	0.01 to 19 GHz
Differential Output Swing	Vin_pp			900	mV	TP4
Eye width		0.57			UI	TP4
Eye height, Differential		228			mV	TP4
Vertical eye closure				5.5	ps	TP4

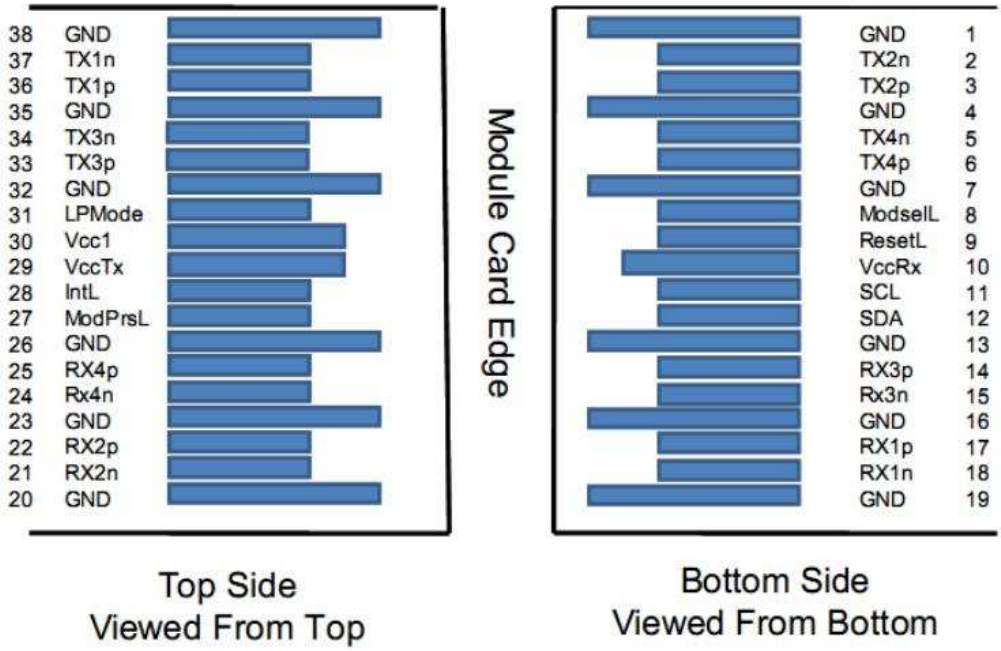
Notes:

1. SDD11≥9.5–0.37f,when 0.01≤f<8 ; SDD11≥ 4.75–7.4log$_{10}$(.f/14), when 8≤f<19

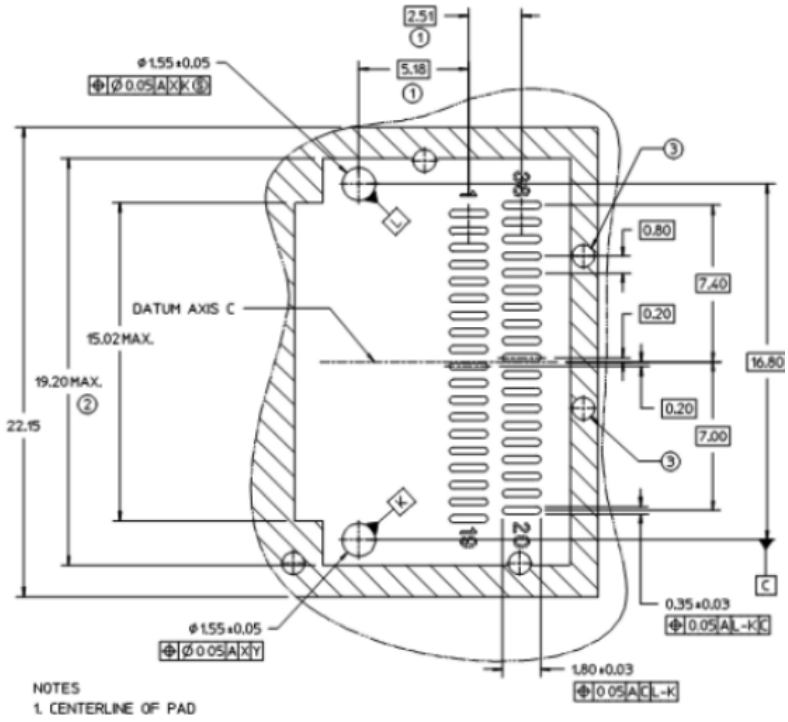
2. SCD11≥22–20(f / 25.78),when 0.01≤f<12.89 ; SDC11≥15–6(f / 25.78),when 12.89≤f<19

8. Pin Description

QSFP Module Pad Layout (Top View)



Host PCB Layout (Top View)



9. Module Electrical Pin Function Definition

Pin	Logic	Symbol	Description	Note
1		GND	Ground	[1]
2	CML-I	Tx2n	Transmitter Inverted Data Input	
3	CML-I	Tx2p	Transmitter Non-inverted Data Input	
4		GND	Ground	[1]
5	CML-I	Tx4n	Transmitter Inverted Data Input	
6	CML-I	Tx4p	Transmitter Non-inverted Data Input	
7		GND	Ground	[1]
8	LVTTL-I	ModSelL	Module Select	
9	LVTTL-I	ResetL	Module Reset	
10		Vcc Rx	+3.3V Power Supply Receiver	
11	LVCMOS-I/O	SCL	2-Wire Serial Interface Clock	[2]
12	LVCMOS-I/O	SDA	2-Wire Serial Interface Data	[2]
13		GND	Ground	[1]
14	CML-O	Rx3p	Receiver Non-Inverted Data Output	
15	CML-O	Rx3n	Receiver Inverted Data Output	

16		GND	Ground	[1]
17	CML-O	Rx1p	Receiver Non-Inverted Data Output	
18	CML-O	Rx1n	Receiver Inverted Data Output	
19		GND	Ground	[1]
20		GND	Ground	[1]
21	CML-O	Rx2n	Receiver Inverted Data Output	
22	CML-O	Rx2p	Receiver Non-Inverted Data Output	
23		GND	Ground	[1]
24	CML-O	Rx4n	Receiver Inverted Data Output	
25	CML-O	Rx4p	Receiver Non-Inverted Data Output	
26		GND	Ground	[1]
27	LVTTL-O	ModPrsL	Module Present	[2]
28	LVTTL-O	IntL	Interrupt	[2]
29		Vcc Tx	+3.3V Power Supply Transmitter	
30		Vcc1	+3.3V Power Supply	
31	LVTTL-I	LPMode	Low Power Mode	
32		GND	Ground	[1]
33	CML-I	Tx3p	Transmitter Non-inverted Data Input	
34	CML-I	Tx3n	Transmitter Inverted Data Input	
35		GND	Ground	[1]
36	CML-I	Tx1p	Transmitter Non-inverted Data Input	
37	CML-I	Tx1n	Transmitter Inverted Data Input	
38		GND	Ground	[1]

Notes:

1.Module ground pins GND are isolated from the module case and chassis ground within the module.

2.Shall be pulled up with 4.7K-10Kohms to a voltage between 3.15V and 3.45V on the host board.

Please refer to SFF-8679 for more information on interface circuit and power filtering network.

10. Low Speed Electrical Hardware Pins

In addition to 2-wire serial interface, the module has the following low speed pins for control and status:

ModSelL, ResetL, LPMode, ModPrsL, IntL

10.1 ModSelL

The ModSelL is an input pin. When held low by the host, the module responds to 2-wire serial communication commands. The ModSelL allows the use of multiple modules on a single 2-wire interface bus. When the ModSelL is "High", the module shall not respond to or acknowledge any 2-wire interface communication from the host. ModSelL signal input node shall be biased to the "High" state in the module. In order to avoid conflicts, the host system shall not attempt 2-wire interface communications within the ModSelL de-assert time after any modules are deselected. Similarly, the host shall wait at least for the period of the ModSelL assert time before communicating with the newly selected module. The assertion and de-asserting periods of different modules may overlap as long as the above timing requirements are met.

10.2 ResetL

The ResetL pin shall be pulled to Vcc in the module. A low level on the ResetL pin for longer than the minimum pulse length (t_Reset_init) initiates a complete module reset, returning all user module settings to their default state. Module Reset Assert Time (t_init) starts on the rising edge after the low level on the ResetL pin is released. During the execution of a reset (t_init) the host shall disregard all status bits until the module indicates a completion of the reset interrupt. The module indicates this by asserting "low" an IntL signal with the Data_Not_Ready bit negated. Note that on power up (including hot insertion) the module should post this completion of reset interrupt without requiring a reset.

10.3 LPMode

The LPMode pin shall be pulled up to Vcc in the module. The pin is a hardware control used to put modules into a low power mode when high. By using the LPMode pin and a combination of the Power_override, Power_set and High_Power_Class_Enable software control bits (Address A0h, byte 93 bits 0,1,2), the host controls how much power a module can dissipate.

10.4 ModPrsL

ModPrsL is pulled up to Vcc_Host on the host board and grounded in the module. The ModPrsL is asserted "Low" when inserted and deasserted "High" when the module is physically absent from the host connector.

10.5 IntL

IntL is an output pin. When IntL is "Low", it indicates a possible module operational fault or a status critical to the host system. The host identifies the source of the interrupt using the 2-wire serial interface. The IntL pin is an open collector output and shall be pulled to host supply voltage on the host board. The INTL pin is deasserted "High" after completion of reset, when byte 2 bit 0 (Data Not Ready) is read with a value of '0' and the flag field is read.

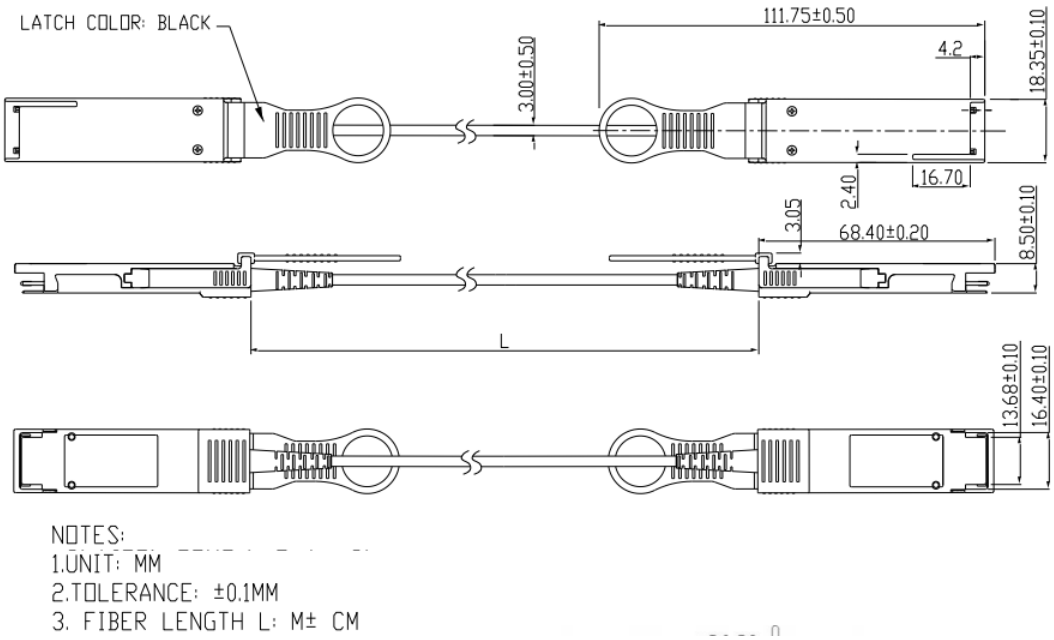
11. Memory Map of Management Interface

The memory map is structured as a single address, multiple page approach. The map is arranged into a single lower page address space of 128 bytes and multiple upper address pages. This structure permits timely access to addresses in the lower page such as interrupt flags and monitors. Less time critical entries such as serial ID information and threshold settings are available with the page select function. Abundant functions will be implemented into WT-QSFP28-AOC-XX for the purpose of monitoring and control. WT-QSFP28-AOC-XX is designed to be compliant to SFF-8636. There are many registers and sophisticated behaviors associated to those functions.

2-Wire Serial Address 1010000x
Lower Page 00h
0 Identifier
1- 2 Status
3- 21 Interrupt Flags
22- 33 Module Monitors
34- 81 Channel Monitors
82- 85 Reserved
86- 98 Control
99 Reserved
100-106 Free Side Device and Channel Mask
107 Reserved
108-112 Free Side Device Properties
113-118 Reserved
119-122 Password Change Entry Area (Optional)
123-126 Password Entry Area (Optional)
127 Page Select Byte

	Optional	**Optional**	**Optional**
Upper Page 00h	**Page 01h**	**Page 02h**	**Page 03h (Cable Assemblies)**
128 Identifier	128 CC_APPS	128-255 User EEPROM Data	128-175 Free Side Device Thresholds
129-191 Base ID Fields	129 AST Table Length (TL)		
	130-131 Application Code Entry 0		
	132-133 Application Code Entry 1		
	134-253 other entries		176-223 Channel Threshold
192-223 Extended ID			224-225 Reserved
224-255 Vendor Specific ID			226-227 Vendor Specific
			238-241 Channel Controls
			242-253 Channel Monitor Masks
	254-255 Application Code Entry TL		254-255 Reserved

12. Mechanical Specification



13. Ordering Information

Model number: WT-QSFP28-AOC-XX

xx □ fiber cable length

03= 3 meters

05= 5 meters

10= 10 meters

25= 25 meters

50= 50 meters

A0= 100 meters

Other= Customized length